We Claim:

1. A method for sealing a thin film transistor comprising the steps of:

(a) providing a thin film transistor comprising a gate electrode, a gate dielectric, a source and a drain electrode, and a semiconductor layer; and

(b) vapor depositing a sealing material on at least a portion of said semiconductor layer through a pattern of an aperture mask.

2. The method of claim 1 wherein said sealing material forms a preselected pattern on at least a portion of said semiconductor layer.

3. The method of claim 1 wherein said sealing material has a resistivity of at least 10x that of said semiconductor layer.

4. The method of claim 1 wherein said sealing material has a resistivity of at least 100x that of said semiconductor layer.

5. The method of claim 1 wherein said sealing material has a resistivity of at least $1x10^6$ ohm-cm.

6. The method of claim 1 wherein said sealing material is a metal oxide, metal nitride, silicon oxide, silicon nitride, or a polymer.

7. The method of claim 6 wherein said polymer is parylene.

8. The method of claim 1 wherein said sealing material is transparent.

9. The method of claim 1 wherein said semiconductor layer is an organic semiconductor.

10. The method of claim 9 wherein said organic semiconductor comprises pentacene or a substituted pentacene.

11. The method of claim 1 wherein said aperture mask is a polymeric aperture mask.

12. The method of claim 9 wherein said thin film transistor further comprises a surface treatment layer interposed between said dielectric layer and said semiconductor layer.

13. The method of claim 1 further comprising the step of vapor depositing a metal layer on said sealing material through said pattern of said aperture mask.

14. The method of claim 1 further comprising the step of interconnecting said thin film transistor to at least one other thin film transistor to form an integrated circuit.

15. The method of claim 1 wherein said thin film transistor is part of an integrated circuit.

16. The method of claim 15 wherein said sealing material covers at least a portion of said integrated circuit.

17. The method of claim 16 wherein said sealing material covers at least a portion of conducting lines of said integrated circuit.

18. A method of making a thin film transistor comprising the steps of:

(a) providing a substrate;

(b) depositing a gate electrode material on said substrate through a pattern of an aperture mask;

(c) depositing a gate dielectric on said gate electrode material through a pattern of an aperture mask;

(d) depositing a semiconductor layer adjacent to said gate dielectric through a pattern of an aperture mask;

(e) depositing a source electrode and a drain electrode contiguous to said semiconductor layer through a pattern of an aperture mask; and

(f) vapor depositing a sealing material on at least a portion of said semiconductor layer through a pattern of an aperture mask.

19. The method of claim 18 wherein at least one of said depositing steps (b) to (e) are vapor depositing steps under vacuum.

20. The method of claim 19 wherein all of said depositing steps (b) to (e) are vapor depositing steps under vacuum.

21. The method of claim 20 wherein the method is carried out in its entirety without breaking vacuum.

22. The method of claim 18 wherein the steps are performed in the order listed.

23. The method of claim 18 wherein said sealing material has a resistivity of at least 10x that of said semiconductor layer.

24. The method of claim 23 wherein said sealing material is transparent.

25. The method of claim 18 wherein said semiconductor layer is an organic semiconductor.

26. The method of claim 25 wherein said organic semiconductor layer comprises pentacene or a substituted pentacene.

27. The method of claim 18 wherein said gate electrode material, gate dielectric, semiconductor layer, source and drain electrodes, and sealing material are deposited through a single aperture mask formed with a pattern of deposition apertures.

28. The method of claim 18 wherein said gate electrode material, gate dielectric, semiconductor layer, source and drain electrodes, and sealing material are each deposited through a separate aperture mask of a mask set.

29. The method of claim 18 further comprising the step of depositing a surface treatment layer between said

dielectric layer and said semiconductor layer.

30. A transistor comprising a substrate, a gate electrode, a gate dielectric, a source and drain electrode, a semiconductor layer, and a vapor deposited sealing layer on at least a portion of said semiconductor layer.